REMARKS

Claims 1-23, all the claims pending in the application, stand rejected upon informalities and prior art grounds. In addition, the drawings are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. Objections to the Drawings

The Office Action argues that the first type of signal and second type of signal defined in the claims are not shown in the drawings. However, Applicants' Figures 2 and 3 illustrate both the first-type signal (where the gate signal 110 rises) and the second-type signal (where the gate signal 110 falls). Therefore, Applicants submit that the drawings clearly illustrate the claimed first-type signal and second-types signal and respectfully request that the drawing objections be removed.

In support of this explanation, Applicants direct the reader's attention to paragraph 15 of the application which explains that the first-type and second-type of signal comprise gating signals applied to the first input of the gating device. These gate signals control whether pulses on the second input of the logical gating device are propagated to the output of the gate device. The first-type of signal allows transitions from the second input to be propagated to the output of the gating device and the second-type of signal prevents the clock pulses from being propagated to the output of the gating device.

Further, paragraph 6 of the application explains that the gate signal 110 enables or blocks the pulses 200, 201 of the clock signal 100. The invention does not modify the timing of the second-types signal (where the gate signal 110 falls), but instead only modifies the timing of the first-type signal (where the gate signal 110 rises). Therefore, Figures 6A and 6B (which explain some of the advantages achieved with the invention) only illustrate different sensing points for the first-type signal. Because the sensing of the second-type signal is not changed with the invention, it is not shown in Figures 6A and 6B (in order to allow the salient features of the

invention to be easily appreciated by the reader); however, as explained above, Figures 2 and 3 clearly illustrate both the first-type and the second-type signals.

In order to match the terminology of the claims exactly with the specification, the claims have been modified to switch the operations of the first-type and second-type signals. However, Applicants respectfully submit that these claim changes merely correct minor inconsistencies between the wording used in the specification (first-type or second-type) with the wording used in the claims (second-type or first-type) and does not broadened or narrow the scope of the invention being defined. Therefore, it is Applicants intention that such claim amendments do not narrow the scope of the claim being defined.

With respect to independent claims 1, 11, and 17, the invention is defined as a method for sensing two different types of signals and "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed." These features are shown in a number of the drawings included in the application. For example, as shown through Figures 6A and 6B, the invention reduces pessimism by reducing the delay calculation within a circuit by reducing the slew (e.g. utilizing factor K). The delay savings can be seen when comparing Figures 6A and 6B. Figure 6A shows a fairly pessimistic situation wherein the midpoint 601 in the slew of the gate signal 110 must occur substantially before the midpoint 600 in the slew of the clock signal 100. The difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 is shown as time period 605. To the contrary, as shown in Figure 6B, by utilizing a sensing point (e.g., "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed" claims 1, 11, and 17) that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements

dramatically. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the drawings.

II. The 35 U.S.C. 112, First Paragraph, Rejection

The Office Action rejects claims 1-23 under 35 U.S.C. § 112, first paragraph, as not being described in the specification or being seen in the drawings. With respect to independent claims 1, 11, and 17, as argued above, the invention is defined as a method for sensing two different types of signals and "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed." These features are shown in a number of the drawings included in the application. For example, applicants' Figures 2 and 3 illustrate both the first-type signal (where the gate signal 110 rises) and the second-type signal (where the gate signal 110 falls). Therefore, Applicants submit that the drawings clearly illustrate the claimed first-type signal and second-types signal and respectfully request that the drawing objections be removed.

In support of this explanation, Applicants direct the reader's attention to paragraph 15 of the application which explains that the first-type and second-type of signal comprise gating signals applied to the first input of the gating device. These gate signals control whether pulses on the second input of the logical gating device are propagated to the output of the gate device. The first-type of signal allows transitions from the second input to be propagated to the output of the gating device and the second-type of signal prevents the clock pulses from being propagated to the output of the gating device.

Further, paragraph 6 of the application explains that the gate signal 110 enables or blocks the pulses 200, 201 of the clock signal 100. The invention does not modify the timing of the second-types signal (where the gate signal 110 falls), but instead only modifies the timing of the first-type signal (where the gate signal 110 rises). Therefore, Figures 6A and 6B (which explain some of the advantages achieved with the invention) only illustrate different sensing points for the first-type signal. Because the sensing of the second-type signal is not changed with the

invention, it is not shown in Figures 6A and 6B (in order to allow the salient features of the invention to be easily appreciated by the reader); however, as explained above, Figures 2 and 3 clearly illustrate both the first-type and the second-type signals.

As shown above, the drawings and specifications fully support and describe the features defined by the claims. Therefore, Applicants respectfully submit that the claims are valid under 35 U.S.C. § 112, first paragraph, and request that this rejection be withdrawn.

III. The Prior Art Rejection

Claims 1-23 stand rejected under 35 U.S.C. §102(a) as being anticipated by Walden (U.S. Patent No. 6,049,236). Applicants respectfully traverse these rejections based on the following discussion.

Walden discloses a clock driving circuit where the on-off frequency can be varied in a controlled manner. However, the timing diagrams in Figures 1B and 4A-6B of Walden clearly illustrate that Walden provides the same sensing operation (and timing) for both the rising gate signal and the falling gate signal. Therefore, unlike the claimed invention, Walden does not distinguish between the timing of the sensing of the rising gate signal and the falling gate signal.

Thus, it is Applicants position that Walden does not teach or suggest the invention defined by independent claims 1, 11, or 17. More specifically, Walden does not teach or suggest "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal and an earlier point in time than said second-type of signal is sensed" as defined by independent claims 1, 11, and 17. Further, Walden is fundamentally unrelated to the invention because Walden does not discussed and is not related to any form of determining or testing (evaluating) gate timing as the invention does. Therefore, it is Applicants position that independent claims 1, 11, and 17 (as well as dependent claims 2-10, 12-16, and 18-23) are patentable over the prior art of record. In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

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IV. Formal Matters and Conclusion

With respect to the objection to claim 3, the spelling error therein has been corrected. Applicants respectfully submit that the forgoing spelling error correction does not broadened or narrow the scope of the claims and it is Applicants intention that the claims not been narrowed by this claim amendment. In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw this objection.

In view of the foregoing, Applicants submit that claims 1-23, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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Marked Up Version Showing Changes Made

1. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal [inhibits] allows transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal [allows] inhibits transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

3. (Amended) The method of claim 1, wherein:

said input comprises a clock input;

said first-type of signal and said second-type of signal comprise clock trailing edge signals;

said first-type of signal [prevents] causes a transition at said output of said gate device due to a transition on a gate [inpit] input of said gate device; and

said second-type of signal [causes] prevents a transition at said output of said gate device.

4. (Amended) The method of claim 2, wherein said first-type of signal [prevents] allows said clock pulses [from being] to be propagated on said output of said gating device and said second-type of signal [allows] prevents said clock pulses [to be] from being propagated on said output of said gating device.

11. (Amended) A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal [inhibits] allows a clock pulse [from being] to be output from said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal [allows] inhibits said clock pulse [to be] from being output from said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

17. (Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal [inhibits] allows transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal [allows] inhibits transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

19. (Amended) The program storage device of claim 18, wherein said first-type of signal [prevents] allows said clock pulses [from being] to be propagated on said output of said gating device and said second-type of signal [allows] prevents said clock pulses [to be] from being propagated on said output of said gating device.